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***INSTITUTE OF INFORMATION TECHNOLOGY***

***JAHANGIRNAGAR UNIVERSITY***

**Number of Assignment :** 03

**Name of Assignment :** Designing Combinational Logic Circuits.

**Course Tittle :** Digital Logic Design

**Course Code :** ICT – 2103

**Submission Date :** 24/12/2020

**Submitted To Submitted By**

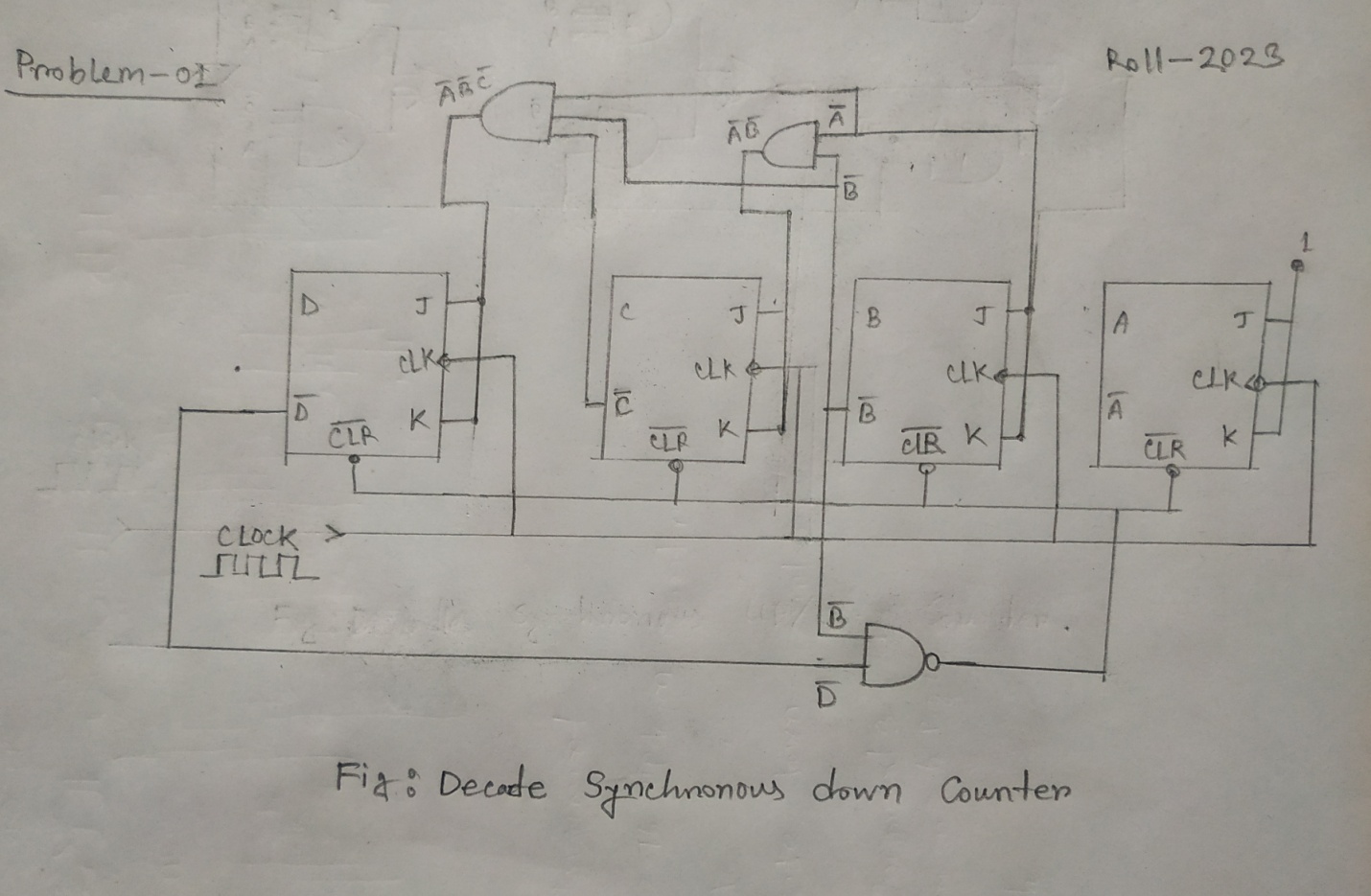
[Dr. Md. Sazzadur Rahman](https://juniv.edu/teachers/rhemel) MD. Shakil Hossain

Assistant Professor Roll – 2023

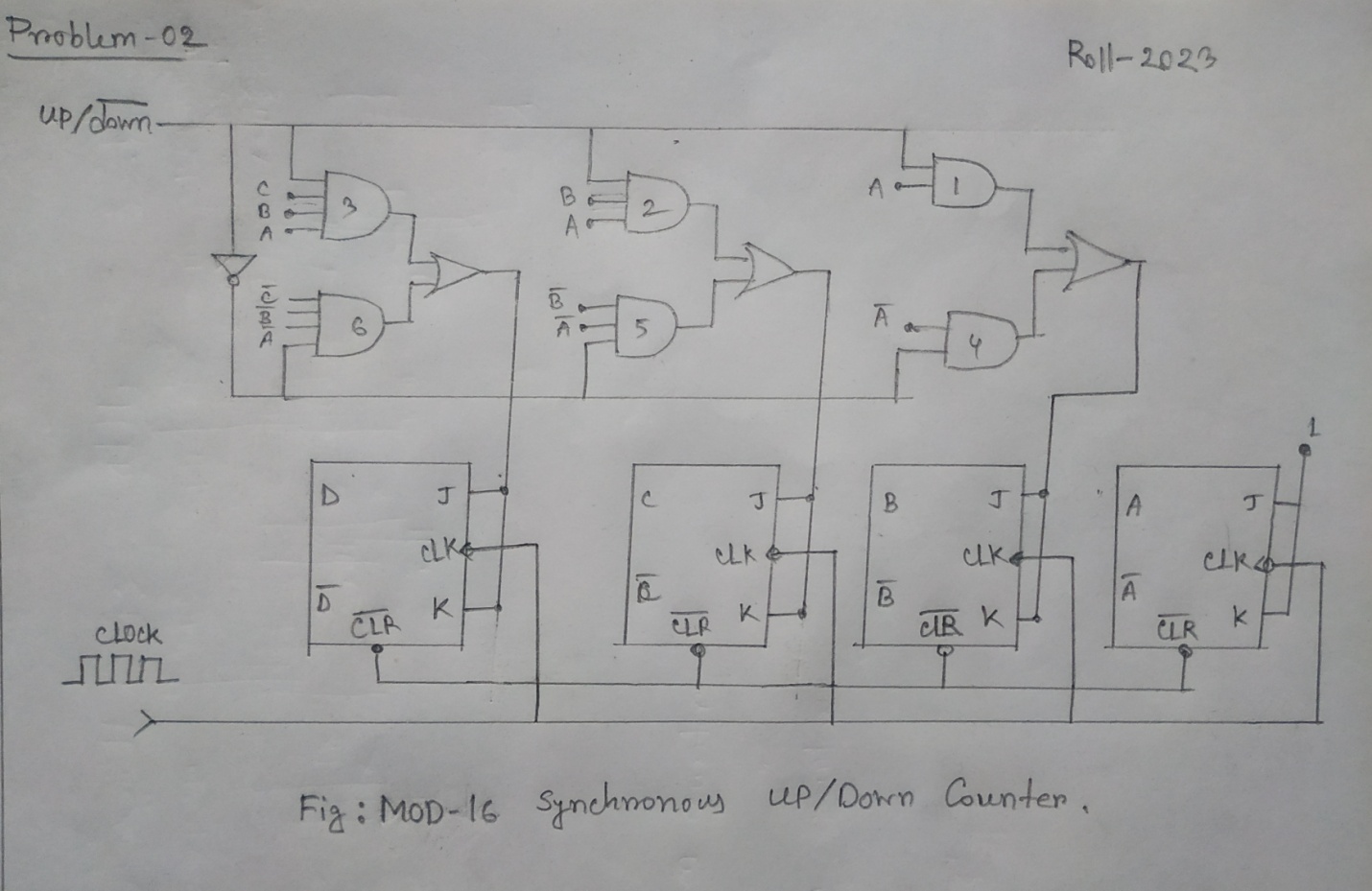
IIT – JU 2nd year 1st Semester

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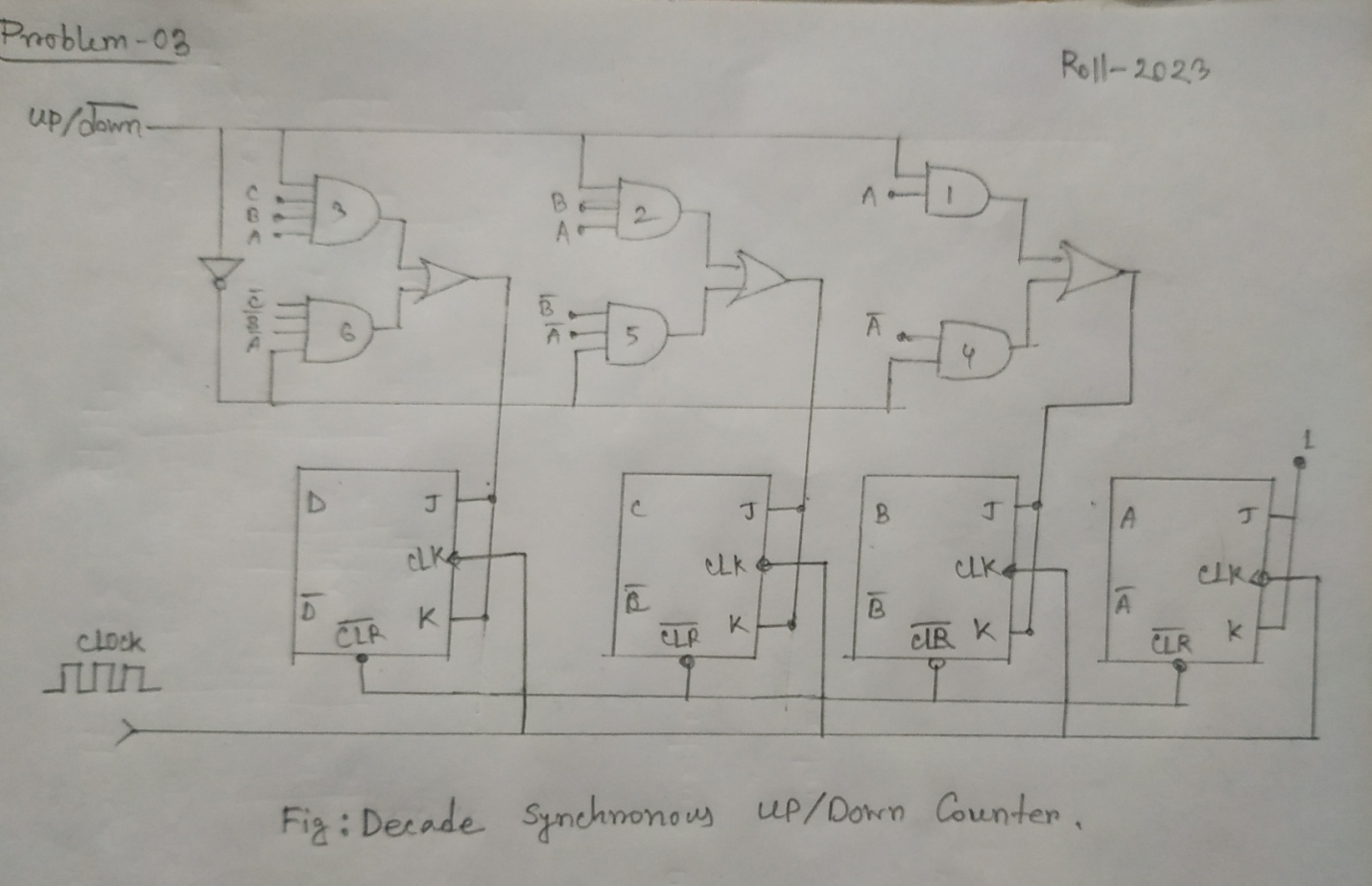
1. Decade synchronous down counter.



2. Mod-16 synchronous up/down counter.

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1. Decade synchronous up/down counter.

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